Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	432	soc and pin and verif$7 and allocat$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:31
L2	118	soc and pin and verif$7 and allocat$5 and mux	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:32
L3	105	soc and pin and verif$7 and allocat$5 and mux and I/O	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:35
L7	319	(verification and circuit and design).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:38
L8	23	(verification and circuit and design).ti. and I/O	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:40
L9	18	(verification and circuit and design).ti. and I/O and (not devins)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:43
L10	319	(verification and circuit and design).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:43
L11	168	(verification and circuit and design and integrated).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/09 19:43